

MOS FIELD EFFECT TRANSISTOR

2SJ449

SWITCHING P-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SJ449 is P-Channel MOS Field Effect Transistor designed for high voltage switching applications.

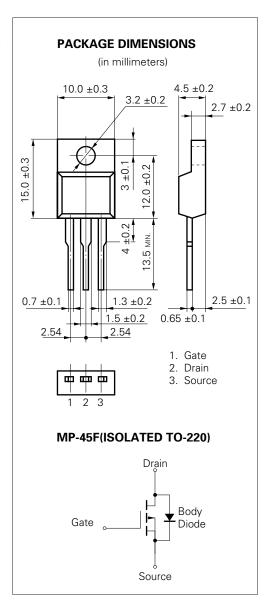
FEATURES

- Low On-Resistance
 - $R_{DS(on)} = 0.8 \Omega MAX$. (@ VGS = -10 V, ID = -3.0 A)
- Low Ciss Ciss = 1040 pF TYP.
- High Avalanche Capability Ratings
- Isolated TO-220 Package

ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

Drain to Source Voltage	VDSS	-250	V
Gate to Source Voltage	Vgss	∓30	V
Drain Current (DC)	ID(DC)	∓6.0	Α
Drain Current (pulse)*	D(pulse)	∓24	Α
Total Power Dissipation ($T_c = 25$ °C)	P _{T1}	35	W
Total Power Dissipation (TA = 25 $^{\circ}$ C)	P _{T2}	2.0	W
Channel Temperature	T_ch	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Single Avalanche Current**	las	-6.0	Α
Single Avalanche Energy**	Eas	180	mJ

- * PW \leq 10 μ s, Duty Cycle \leq 1 %
- ** Starting Tch = 25 °C, Rg = 25 Ω , Vgs = -20 V \rightarrow 0



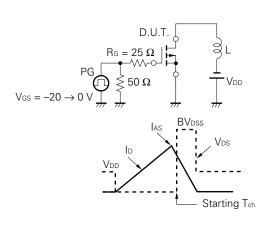


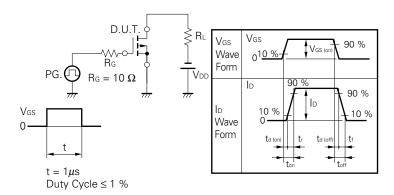
ELECTRICAL CHARACTERISTICS (TA = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	RDS(on)		0.55	0.8	Ω	Vgs = -10 V, ID = -3.0 A
Gate to Source Cutoff Voltage	V _{GS(off)}	-4.0	-4.8	-5.5	V	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$
Forward Transfer Admittance	yfs	2.0	3.5		S	$V_{DS} = -10 \text{ V}, I_{D} = -3.0 \text{ A}$
Drain Leakage Current	IDSS			-100	μΑ	V _{DS} = -250 V, V _{GS} = 0
Gate to Source Leakage Current	Igss			∓100	nA	V _G S = ∓30 V, V _D S = 0
Input Capacitance	Ciss		1040		pF	V _{DS} = -10 V
Output Capacitance	Coss		360		pF	V _G s = 0
Reverse Transfer Capacitance	Crss		70		pF	f = 1 MHz
Turn-On Delay Time	td(on)		24		ns	ID = -3.0 A
Rise Time	tr		16		ns	$V_{GS(on)} = -10 \text{ V}$
Turn-Off Delay Time	td(off)		47		ns	V _{DD} = -125 V
Fall Time	tf		14		ns	Rg = 10 Ω , RL = 42 Ω
Total Gate Charge	Qg		23.1		nC	ID = -6.0 A
Gate to Source Charge	Qgs		7.1		nC	V _{DD} = -200 V
Gate to Drain Charge	QGD		12.9		nC	V _G S = -10 V
Body Diode Forward Voltage	V _F (S-D)		0.92		V	IF = -6.0 A, VGS = 0
Reverse Recovery Time	trr		155		ns	IF = -6.0 A, VGS = 0
Reverse Recovery Charge	Qrr		930		nC	$di/dt = 50 A/\mu s$

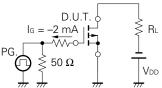
Test Circuit 1 Avalanche Capability

Test Circuit 2 Switching Time



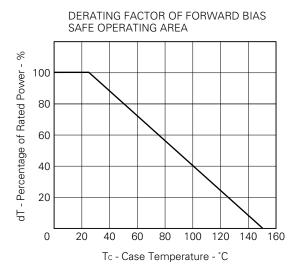


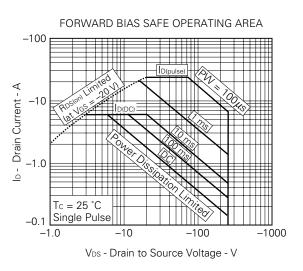
Test Circuit 3 Gate Charge

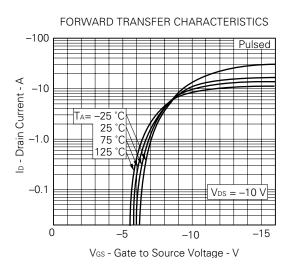


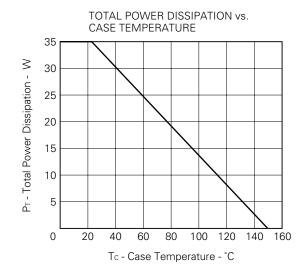
The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

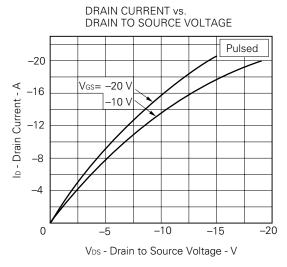
TYPICAL CHARACTERISTICS (TA = 25 °C)





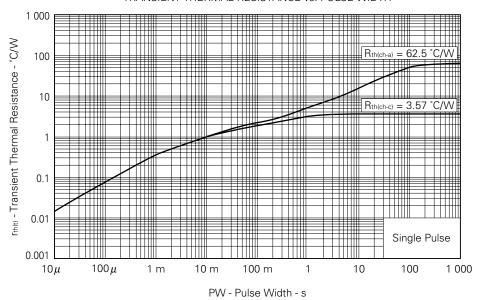




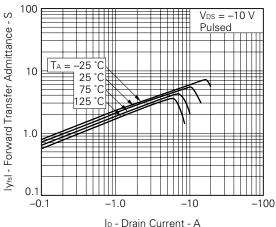


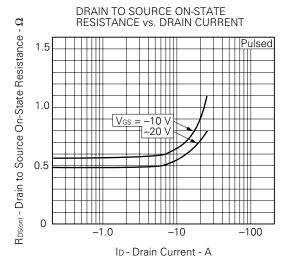
NEC

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

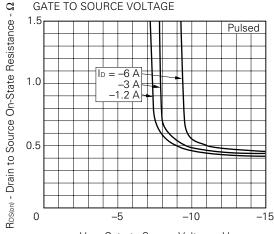






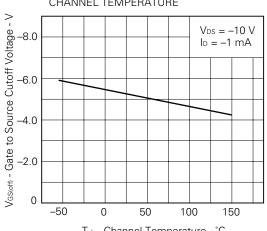


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



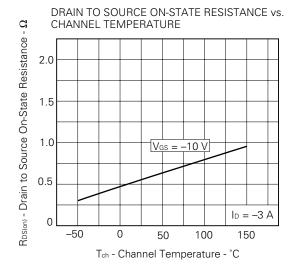
Vgs - Gate to Source Voltage - V

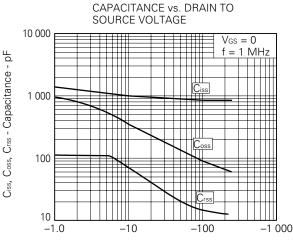
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

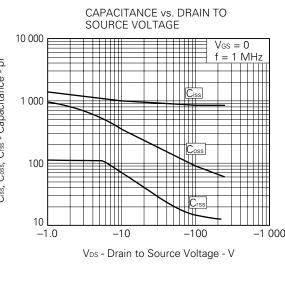


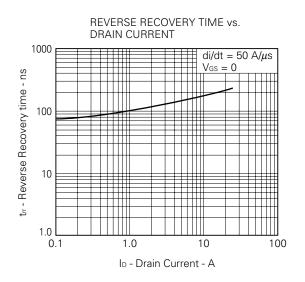
 T_ch - Channel Temperature - ${}^\circ\mathsf{C}$

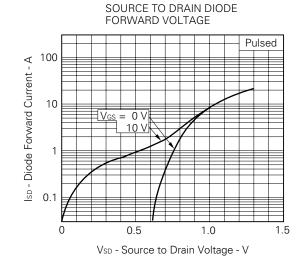


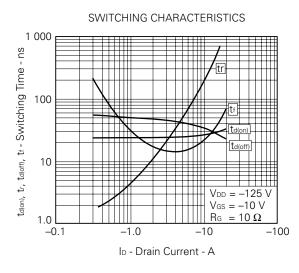


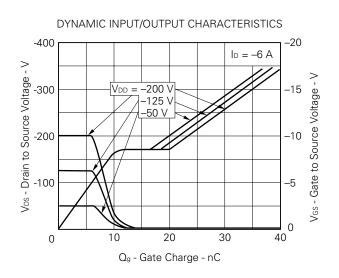




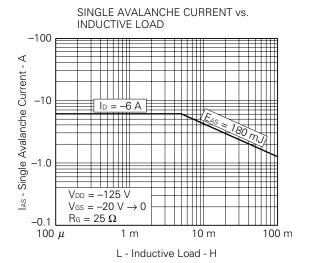


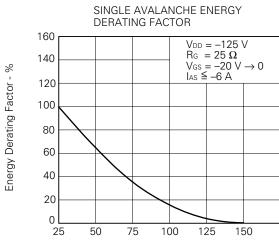












Starting Tch - Starting Channel Temperature - $^{\circ}\text{C}$



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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