

SN54ALS00A, SN54AS00, SN74ALS00A, SN74AS00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

SDAS187A – APRIL 1982 – REVISED DECEMBER 1994

- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

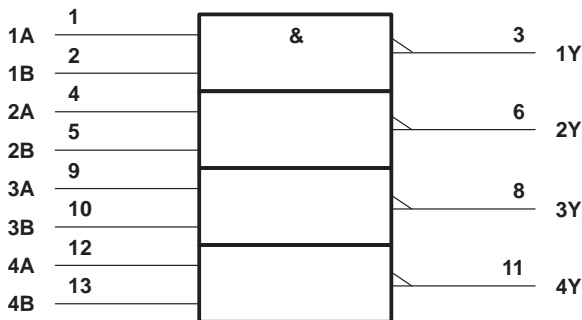
These devices contain four independent 2-input positive-NAND gates. They perform the Boolean functions $Y = \overline{A} \cdot B$ or $Y = \overline{A + B}$ in positive logic.

The SN54ALS00A and SN54AS00 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS00A and SN74AS00 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE
(each gate)

| INPUTS | | OUTPUT Y |
|--------|---|-------------|
| A | B | |
| H | H | L |
| L | X | H |
| X | L | H |

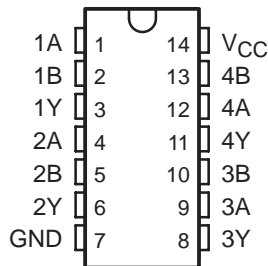
logic symbol†



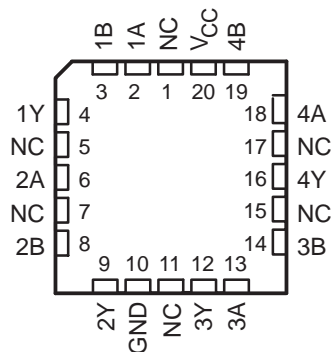
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

SN54ALS00A, SN54AS00 . . . J PACKAGE
SN74ALS00A, SN74AS00 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS00A, SN54AS00 . . . FK PACKAGE
(TOP VIEW)

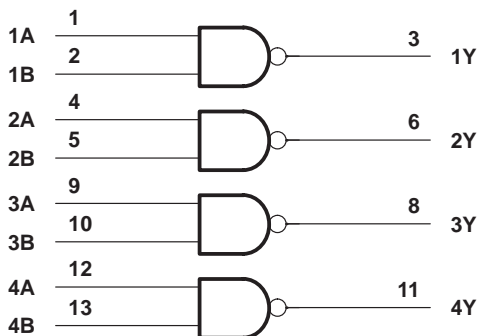


NC – No internal connection

SN54ALS00A, SN54AS00, SN74ALS00A, SN74AS00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Operating free-air temperature range, T_A : SN54ALS00A | -55°C to 125°C |
| SN74ALS00A | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | SN54ALS00A | | | SN74ALS00A | | | UNIT |
|--------------------------------------|------------|-----|------|------------|-----|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V_{IH} High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} Low-level input voltage | | | 0.8‡ | | | 0.8 | V |
| | | | 0.7§ | | | | |
| I_{OH} High-level output current | | | -0.4 | | | -0.4 | mA |
| I_{OL} Low-level output current | | | 4 | | | 8 | mA |
| T_A Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

‡ Applies over temperature range -55°C to 70°C

§ Applies over temperature range 70°C to 125°C



SN54ALS00A, SN54AS00, SN74ALS00A, SN74AS00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN54ALS00A | | SN74ALS00A | | UNIT | | |
|-----------------|---|--------------|------------------------|------------|--------------|------|---------------|-----|
| | | MIN | TYP† | MAX | MIN | | TYP† | MAX |
| V_{IK} | $V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$ | | | -1.2 | | -1.5 | V | |
| V_{OH} | $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$ | $V_{CC} - 2$ | | | $V_{CC} - 2$ | | V | |
| V_{OL} | $V_{CC} = 4.5\text{ V}$ | | $I_{OL} = 4\text{ mA}$ | 0.25 | 0.4 | 0.25 | 0.4 | V |
| | | | $I_{OL} = 8\text{ mA}$ | | | 0.35 | 0.5 | |
| I_I | $V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$ | | | 0.1 | | 0.1 | mA | |
| I_{IH} | $V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$ | | | 20 | | 20 | μA | |
| I_{IL} | $V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$ | | | -0.1 | | -0.1 | mA | |
| $I_{O\ddagger}$ | $V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$ | -20 | | -112 | -30 | -112 | mA | |
| I_{CCH} | $V_{CC} = 5.5\text{ V}$, $V_I = 0$ | | 0.5 | 0.85 | | 0.5 | 0.85 | mA |
| I_{CCL} | $V_{CC} = 5.5\text{ V}$, $V_I = 4.5\text{ V}$ | | 1.5 | 3 | | 1.5 | 3 | mA |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, $T_A = \text{MIN to MAX}\S$ | | | | UNIT |
|-----------|--------------|-------------|--|-----|------------|-----|------|
| | | | SN54ALS00A | | SN74ALS00A | | |
| | | | MIN | MAX | MIN | MAX | |
| t_{PLH} | A or B | Y | 3 | 15 | 3 | 11 | ns |
| t_{PHL} | | | 2 | 9 | 2 | 8 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS00A, SN54AS00, SN74ALS00A, SN74AS00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

SDAS187A – APRIL 1982 – REVISED DECEMBER 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Operating free-air temperature range, T_A : SN54AS00 | -55°C to 125°C |
| SN74AS00 | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | | SN54AS00 | | | SN74AS00 | | | UNIT |
|----------|--------------------------------|----------|-----|-----|----------|-----|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I_{OH} | High-level output current | | | -2 | | | -2 | mA |
| I_{OL} | Low-level output current | | | 20 | | | 20 | mA |
| T_A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN54AS00 | | | SN74AS00 | | | UNIT |
|-----------|---|--------------|------|------|--------------|------|------|------|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V_{IK} | $V_{CC} = 4.5 V$, $I_I = -18 mA$ | | | -1.2 | | | -1.2 | V |
| V_{OH} | $V_{CC} = 4.5 V$ to $5.5 V$, $I_{OH} = -2 mA$ | $V_{CC} - 2$ | | | $V_{CC} - 2$ | | | V |
| V_{OL} | $V_{CC} = 4.5 V$, $I_{OL} = 20 mA$ | 0.35 | 0.5 | | 0.35 | 0.5 | | V |
| I_I | $V_{CC} = 5.5 V$, $V_I = 7 V$ | | 0.1 | | | 0.1 | | mA |
| I_{IH} | $V_{CC} = 5.5 V$, $V_I = 2.7 V$ | | 20 | | | 20 | | μA |
| I_{IL} | $V_{CC} = 5.5 V$, $V_I = 0.4 V$ | | -0.5 | | | -0.5 | | mA |
| $I_{OS}§$ | $V_{CC} = 5.5 V$, $V_O = 2.25 V$ | -30 | -112 | | -30 | -112 | | mA |
| I_{CCH} | $V_{CC} = 5.5 V$, $V_I = 0$ | | 2 | 3.2 | | 2 | 3.2 | mA |
| I_{CCL} | $V_{CC} = 5.5 V$, $V_I = 4.5 V$ | | 10.8 | 17.4 | | 10.8 | 17.4 | mA |

‡ All typical values are at $V_{CC} = 5 V$, $T_A = 25°C$.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

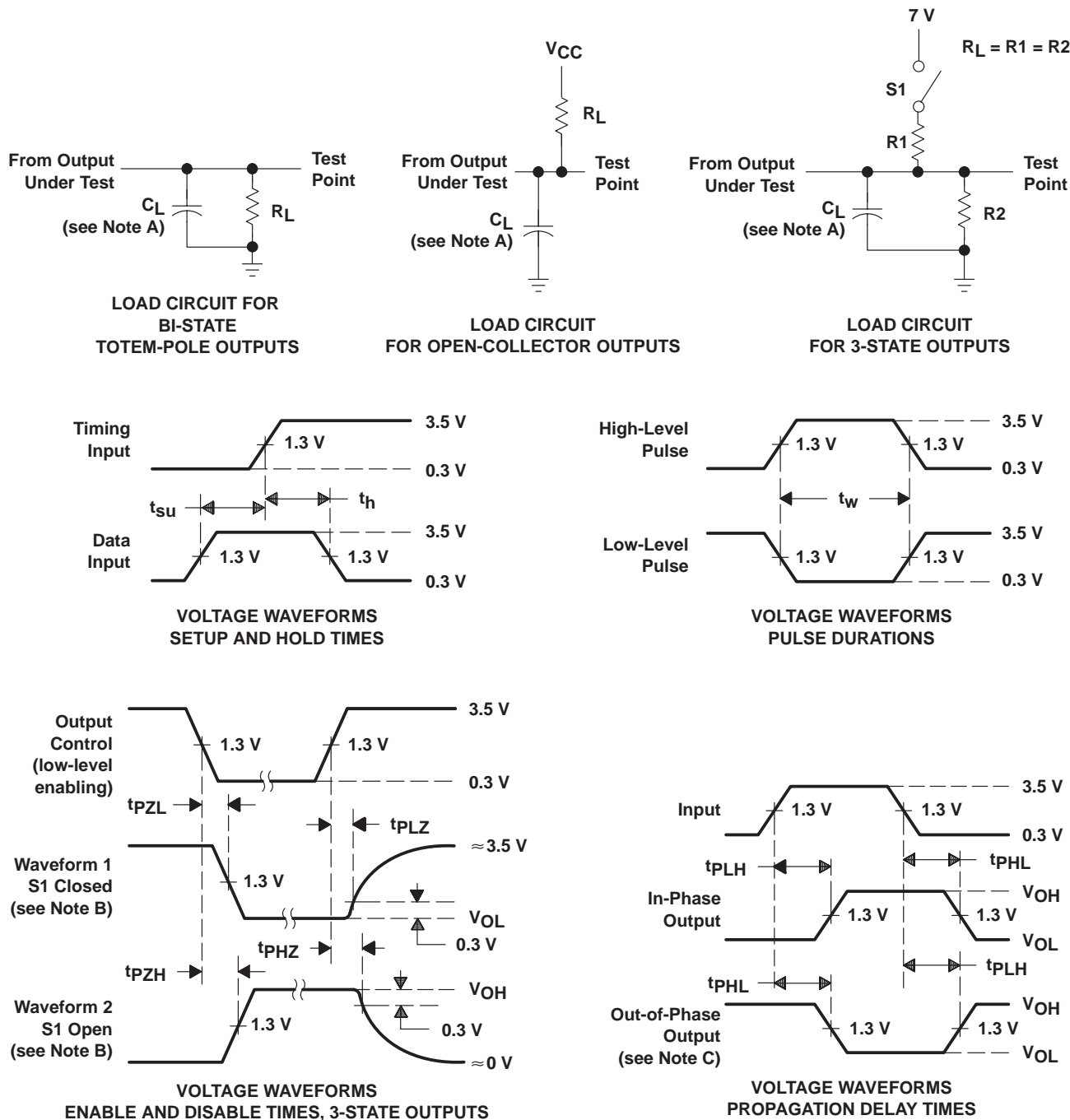
switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 4.5 V$ to $5.5 V$, $C_L = 50 pF$, $R_L = 500 \Omega$, $T_A = MIN$ to MAX ¶ | | | | UNIT |
|-----------|--------------|-------------|--|-----|----------|-----|------|
| | | | SN54AS00 | | SN74AS00 | | |
| | | | MIN | MAX | MIN | MAX | |
| t_{PLH} | A or B | Y | 1 | 5 | 1 | 4.5 | ns |
| t_{PHL} | | | 1 | 5 | 1 | 4 | |

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



PARAMETER MEASUREMENT INFORMATION
 SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|---|-------------------------|
| 5962-86833012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 86833012A SNJ54ALS 00AFK | Samples |
| 5962-8683301DA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8683301DA SNJ54ALS00AW | Samples |
| JM38510/37001B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 37001B2A | Samples |
| JM38510/37001BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 37001BCA | Samples |
| M38510/37001B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 37001B2A | Samples |
| M38510/37001BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 37001BCA | Samples |
| SN54ALS00AJ | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54ALS00AJ | Samples |
| SN54AS00J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54AS00J | Samples |
| SN74ALS00AD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS00A | Samples |
| SN74ALS00ADBR | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | G00A | Samples |
| SN74ALS00ADG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS00A | Samples |
| SN74ALS00ADR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS00A | Samples |
| SN74ALS00ADRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS00A | Samples |
| SN74ALS00ADRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS00A | Samples |
| SN74ALS00AN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS00AN | Samples |
| SN74ALS00AN3 | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74ALS00ANE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS00AN | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|---------------------------------|-------------------------|
| SN74ALS00ANSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS00A | Samples |
| SN74AS00D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS00 | Samples |
| SN74AS00DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS00 | Samples |
| SN74AS00DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS00 | Samples |
| SN74AS00N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS00N | Samples |
| SN74AS00NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS00N | Samples |
| SN74AS00NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74AS00 | Samples |
| SNJ54ALS00AFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-86833012A SNJ54ALS00AFK | Samples |
| SNJ54ALS00AJ | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54ALS00AJ | Samples |
| SNJ54ALS00AW | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8683301DA SNJ54ALS00AW | Samples |
| SNJ54AS00FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ54AS00FK | Samples |
| SNJ54AS00J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54AS00J | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54ALS00A, SN54AS00, SN74ALS00A, SN74AS00 :

● Catalog: [SN74ALS00A](#), [SN74AS00](#)

● Military: [SN54ALS00A](#), [SN54AS00](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALS00ADBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ALS00ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74ALS00ANSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AS00DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74AS00NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALS00ADBR | SSOP | DB | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74ALS00ADR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74ALS00ANSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74AS00DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74AS00NSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.



4040049/E 12/2002

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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