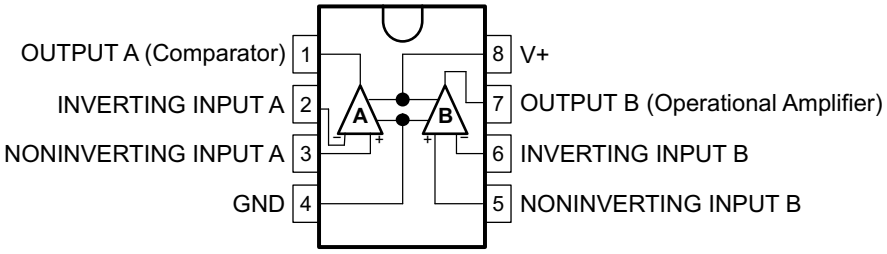
FEATURES

- **Wide Power-Supply Voltage Range**
  - **Single Supply: 3 V to 32 V**
  - **Dual Supply: ±1.5 V to ±16 V**
- **Low Supply-Current Drain Essentially Independent of Supply Voltage: 600 μA**
- **Low Input Biasing Current: 50 nA**
- **Low Input Offset Voltage: 2 mV**
- **Low Input Offset Current: 5 nA**
- **Input Common-Mode Voltage Range Includes Ground**
- **Differential Input Voltage Range Equals Power-Supply Voltage**
- **Additional Operational Amplifier Features**
  - **Internally Frequency Compensated for Unity Gain**
  - **Large DC Voltage Gain: 100 dB**
  - **Wide Bandwidth (Unity Gain): 1 MHz**
  - **Large Output Voltage Swing: 0 V to V+ – 1.5 V**
- **Additional Comparator Features**
  - **Low Output Saturation Voltage: 250 mV at 4 mA**
  - **Output Voltage Compatible With All Types of Logic Systems**

ADVANTAGES

- **Eliminates Need for Dual Power Supplies**
- **An Internally Compensated Operational Amplifier and a Precision Comparator in the Same Package**
- **Allows Sensing at or Near Ground**

D, DGK, OR P PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The LM392 consists of two independent building-block circuits. One is a high-gain internally-frequency-compensated operational amplifier, and the other is a precision voltage comparator. Both the operational amplifier and the voltage comparator are designed to operate from a single power supply over a wide range of voltages. Both circuits have input stages that force the common-mode input down to ground when operating from a single power supply. Operation from split power supplies also is possible, and the low power-supply current is independent of the magnitude of the supply voltage.

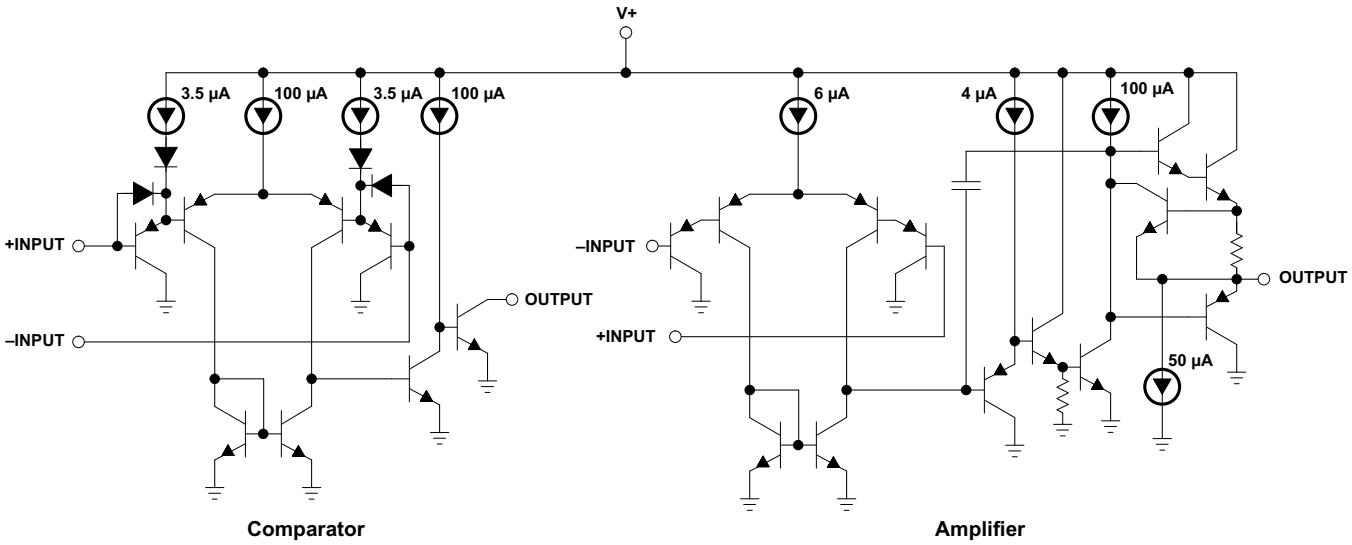
Applications include transducer amplifiers with pulse shapers, DC gain blocks with level detectors, and VCOs, as well as all conventional operational amplifier or voltage-comparator circuits. The LM392 can be operated directly from the standard 5-V power-supply voltage used in digital systems, and the output of the comparator interfaces directly with either TTL or CMOS logic. In addition, the low-power drain makes the LM392 extremely useful in the design of portable equipment.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	MSOP – DGK	Reel of 250	LM392DGKT	PREVIEW
		Reel of 2500	LM392DGKR	
	PDIP – P	Tube of 50	LM392P	LM392P
	SOIC – D	Tube of 75	LM392D	LM392
		Reel of 2500	LM392DR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

SCHEMATIC DIAGRAM



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V+	Supply voltage	Single supply		32	V
		Dual supply		±16	
V_{ID}	Differential input voltage			32	V
V_{IN}	Input voltage range		–0.3	32	V
I_I	Input current(2)	V_{IN} < –0.3 V		50	mA
t_{short}	Duration of output short circuit to ground(3)			Continuous	
θ_{JA}	Package thermal impedance, junction to free air(4)	D package		97	°C/W
		DGK package		172	
		P package		84	
T_{lead}	Lead temperature during soldering	10 s maximum		260	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) This input current exists only when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the device. This transistor action can cause the output voltages of the amplifiers to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive, and normal output states reestablish when the input voltage, which was negative, again returns to a value greater than –0.3 V (at 25°C).

(3) Short circuits from the output to V+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA for the operational amplifier and 30 mA for the comparator, independent of the magnitude of V+. At values of supply voltage in excess of 15 V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.

(4) Package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	MAX	UNIT
V+	Supply voltage	Single supply	3	32	V
		Dual supply	±1.5	±16	
T_A	Operating free-air temperature		0	70	°C

Electrical Characteristics

V+ = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	At output switch point, $V_O \approx 1.4$ V, $R_S = 0\ \Omega$, V+ = 5 V to 30 V, V_{CM} = 0 V to (V+ – 1.5 V)		25°C		±2	±5	mV
				0°C to 70°C			±7	
I_{IB}	Input bias current	IN(+) or IN(–), V_{CM} = 0 V(1)		25°C		50	205	nA
		IN(+) or IN(–)		0°C to 70°C			400	
I_{IO}	Input offset current	IN(+) – IN(–)		25°C		±5	±50	nA
				0°C to 70°C			150	
V_{CM}	Input common-mode voltage(2)	V+ = 30 V		25°C	0		V+ – 1.5	V
				0°C to 70°C	0		V+ – 2	
I+	Supply current	$R_L = \infty$	V+ = 30 V	0°C to 70°C		1	2	mA
			V+ = 5 V			0.5	1	
	Amplifier-to-amplifier coupling	f = 1 kHz to 20 kHz, Input referred(3)		25°C		–100		dB
V_{DI}	Differential input voltage	All $V_{IN} \geq 0$ V (or V–, if used)(4)		0°C to 70°C			32	V

(1) The direction of the input current is out of the device due to the PNP input stage. This current essentially is constant and independent of the state of the output, so no loading change exists on the input lines.
(2) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V+ – 1.5 V, but either or both inputs can go to 32 V without damage.
(3) Due to proximity of external components, ensure that coupling is not originating via the stray capacitance between these external parts. This typically can be detected, as this type of capacitive coupling increases at higher frequencies.
(4) Positive excursions of input voltage may exceed the power-supply level. As long as the other input voltage remains within the common-mode range, the comparator provides a proper output state. The input voltage to the operational amplifier should not exceed the power-supply level. The input voltage state must not be less than –0.3 V (or 0.3 V below the magnitude of the negative power supply, if used) on either amplifier.

Electrical Characteristics, Operational Amplifier Only

V+ = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
A_{VD}	Large signal voltage gain	V+ = 15 V, V_O swing = 1 V to 11 V, $R_L = 2\ k\Omega$		25°C	25	100		V/mV
V_{OS}	Output voltage swing	$R_L = 2\ k\Omega$		25°C	0		V+ – 1.5	V
CMRR	Common-mode rejection ratio	V_{CM} = 0 V to (V+ – 1.5 V)		25°C	65	70		dB
k_{SVR}	Power-supply rejection ratio			25°C	65	100		dB
I_{source}	Output source current	$V_{IN(+)}$ = 1 V, $V_{IN(–)}$ = 0 V, V+ = 15 V, V_O = 2 V		25°C	20	40		mA
I_{sink}	Output sink current	$V_{IN(–)}$ = 1 V, $V_{IN(+)}$ = 0 V, V+ = 15 V	V_O = 2 V	25°C	10	20		mA
			V_O = 200 mV		12	50		µA
αV_{IO}	Input offset voltage drift	$R_S = 0\ \Omega$		0°C to 70°C		7		µV/°C
αI_{IO}	Input offset current drift	$R_S = 0\ \Omega$		0°C to 70°C		10		pA/°C

Electrical Characteristics, Comparator Only

V+ = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_G	Voltage gain	$R_L \geq 15\ k\Omega$, V+ = 15 V		25°C	50	200		V/mV
t_{LSR}	Large signal response time	V_{IN} = TTL logic swing, V_{REF} = 1.4 V, V_{RL} = 5 V, R_L = 5.1 kΩ		25°C		300		ns
t_R	Response time	V_{RL} = 5 V, R_L = 5.1 kΩ		25°C		1.3		µs
I_{sink}	Output sink current	$V_{IN(-)}$ = 1 V, $V_{IN(+)}$ = 0 V, $V_O \geq 1.5$ V		25°C	6	16		mA
V_S	Saturation voltage	$V_{IN(-)} \geq 1$ V, $V_{IN(+)}$ = 0, $I_{SINK} \leq 4$ mA		25°C		250	400	mV
				0°C to 70°C			700	
I_{LO}	Output leakage current	$V_{IN(-)}$ = 0, $V_{IN(+)} \geq 1$ V	V_O = 5 V	25°C		0.1		nA
			V_O = 30 V	0°C to 70°C			1	µA

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM392D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM392	Samples
LM392DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM392	Samples
LM392DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	M7L	Samples
LM392DGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	M7L	Samples
LM392DGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	M7L	Samples
LM392DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	LM392	Samples
LM392DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM392	Samples
LM392P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LM392P	Samples
LM392PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LM392P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

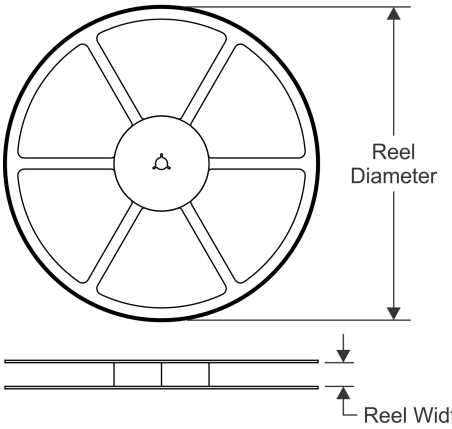
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

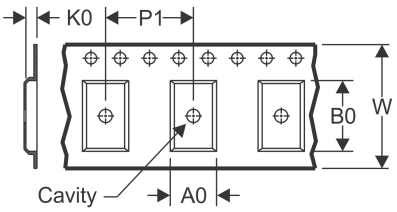
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

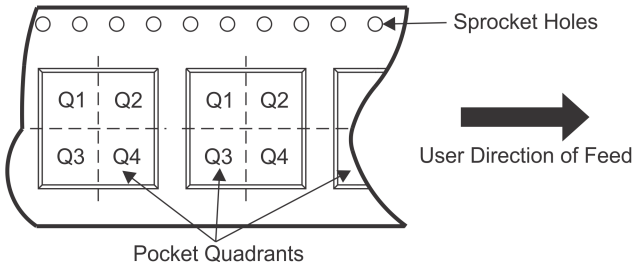


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

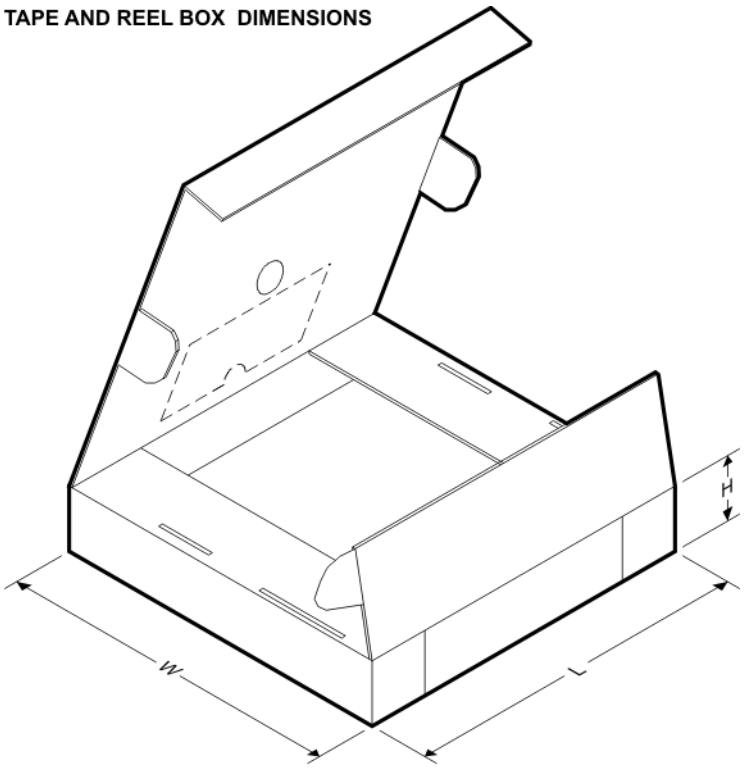
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM392DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM392DGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM392DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM392DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM392DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

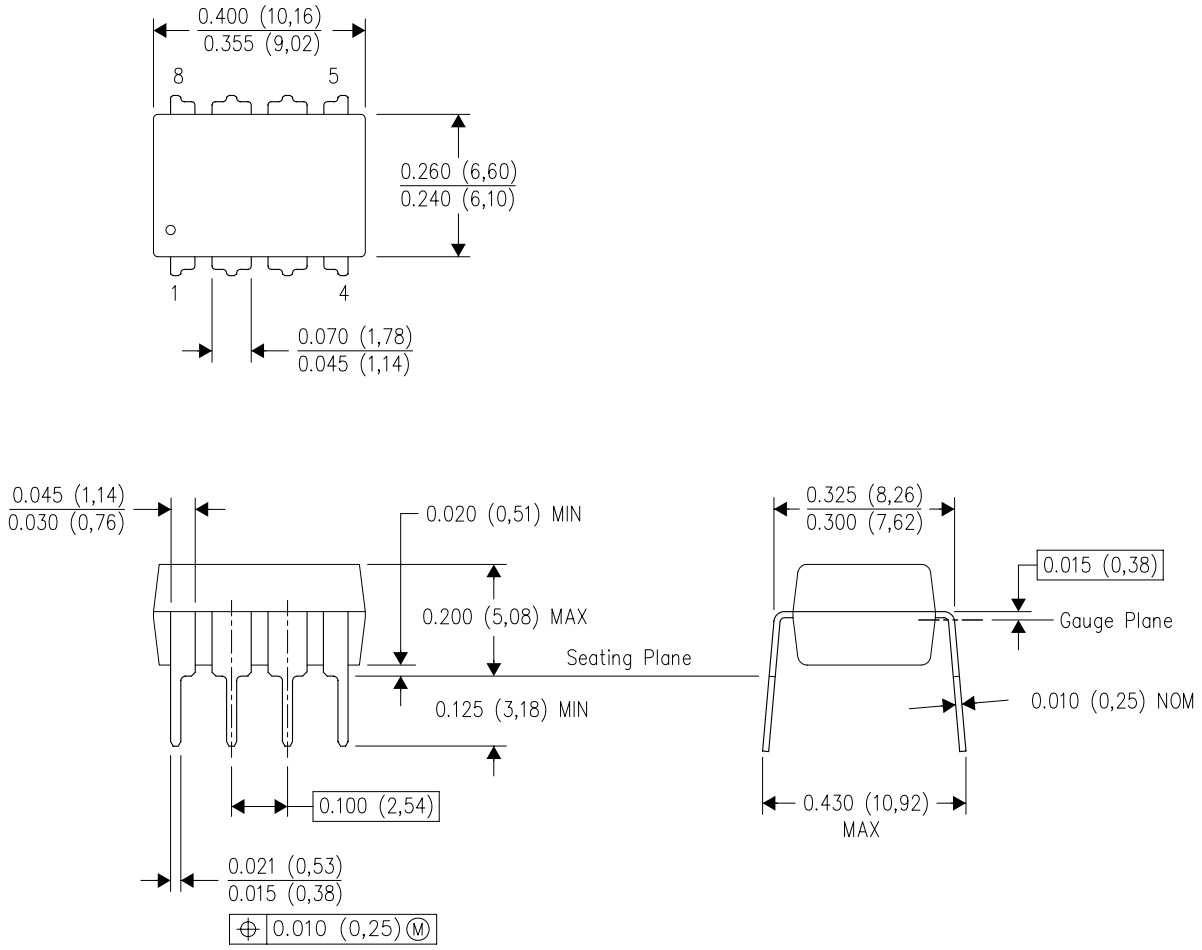
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

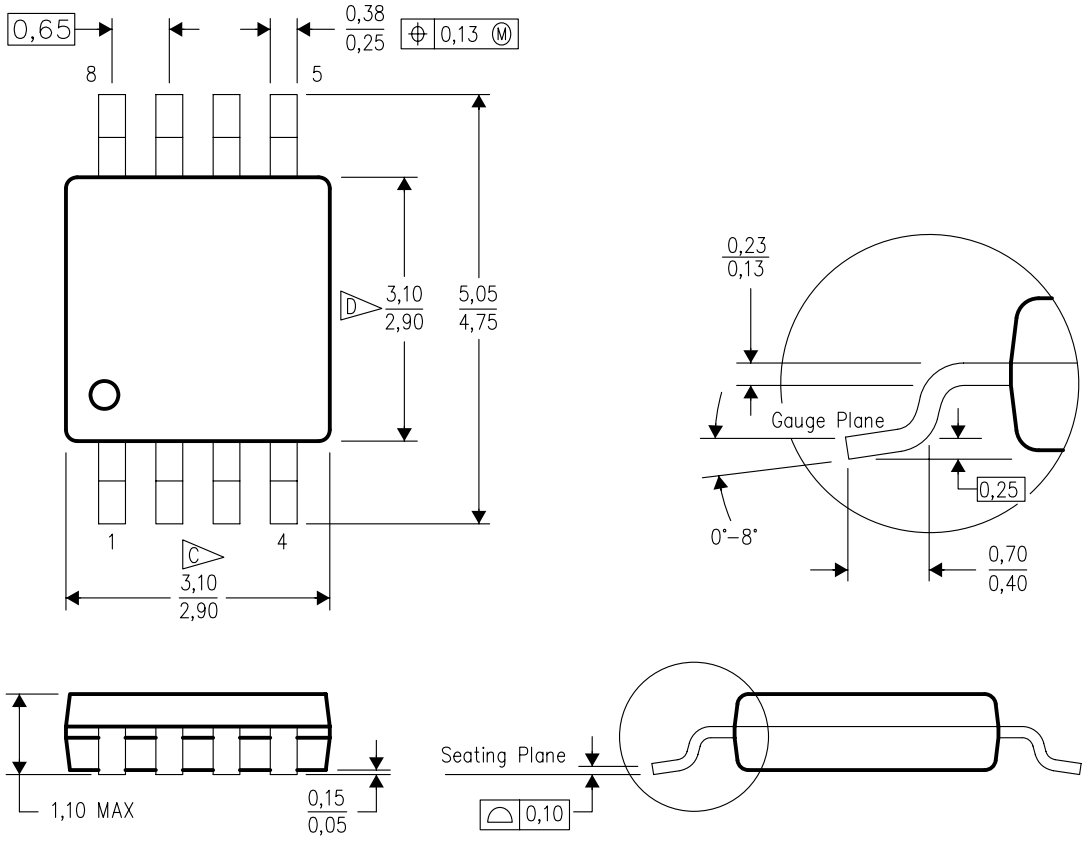
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM392DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LM392DGKT	VSSOP	DGK	8	250	202.0	201.0	28.0
LM392DR	SOIC	D	8	2500	340.5	338.1	20.6
LM392DR	SOIC	D	8	2500	364.0	364.0	27.0
LM392DRG4	SOIC	D	8	2500	340.5	338.1	20.6

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

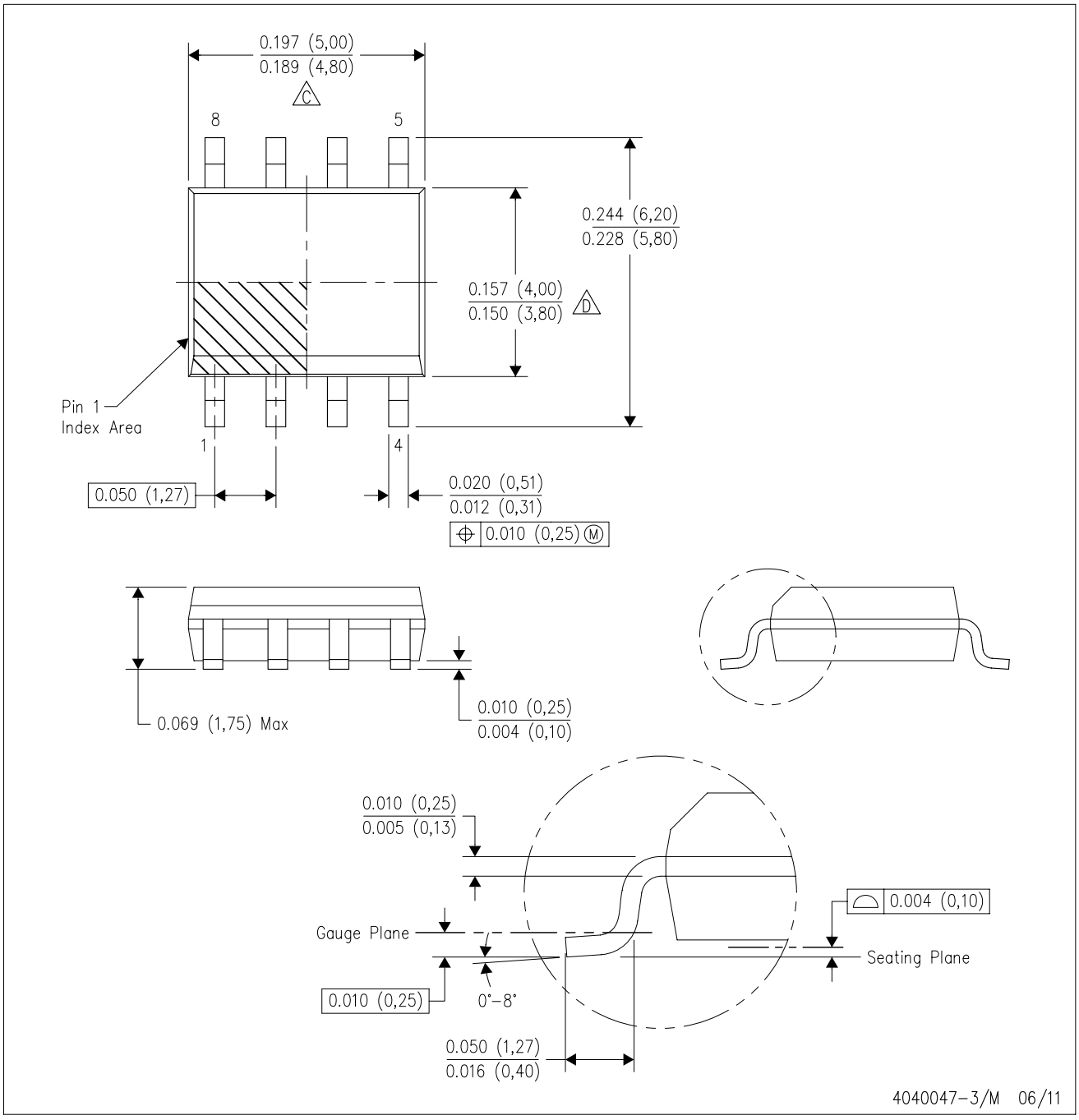
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

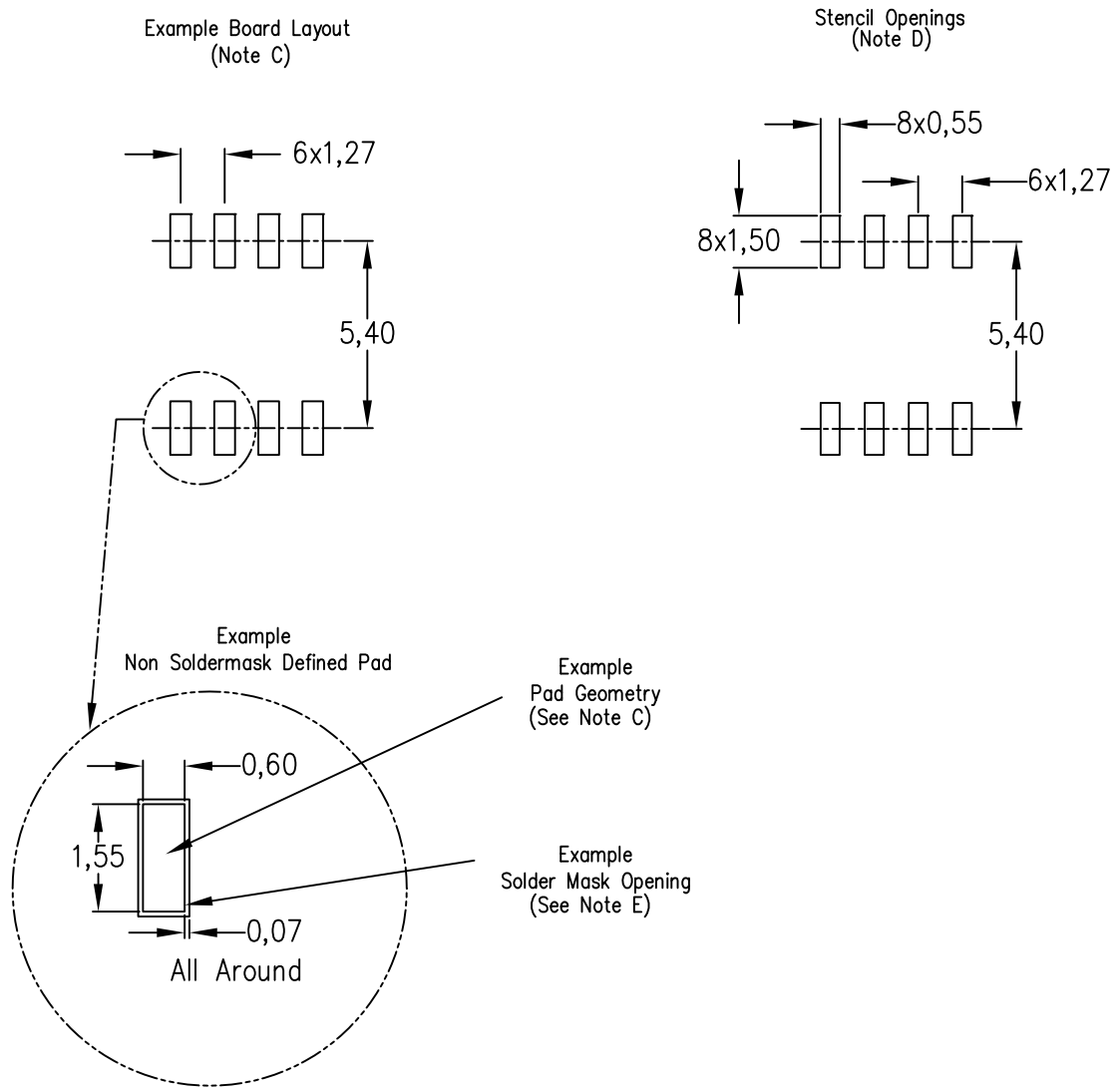
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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