



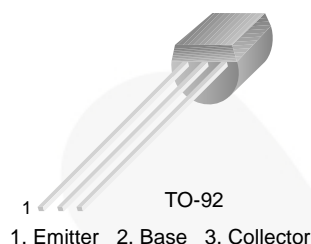
November 2014

SS8550

PNP Epitaxial Silicon Transistor

Features

- 2 W Output Amplifier of Portable Radios in Class B Push-pull Operation.
- Complimentary to SS8050
- Collector Current: $I_C = 1.5 \text{ A}$



Ordering Information

Part Number	Top Mark	Package	Packing Method
SS8550BBU	S8550	TO-92 3L	Bulk
SS8550CBU	S8550	TO-92 3L	Bulk
SS8550CTA	S8550	TO-92 3L	Ammo
SS8550DBU	S8550	TO-92 3L	Bulk
SS8550DTA	S8550	TO-92 3L	Ammo

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage	-40	V
V_{CEO}	Collector-Emitter Voltage	-25	V
V_{EBO}	Emitter-Base Voltage	-6	V
I_C	Collector Current	-1.5	A
T_J	Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-65 to 150	$^\circ\text{C}$

Thermal Characteristics⁽¹⁾

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit
P_D	Power Dissipation	1	W
	Derate Above 25°C	8	mW/ $^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	125	$^\circ\text{C}/\text{W}$

Note:

1. PCB size: FR-4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

Electrical Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{CBO}	Collector-Base Breakdown Voltage	$I_C = -100 \mu\text{A}$, $I_E = 0$	-40			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	$I_C = -2 \text{ mA}$, $I_B = 0$	-25			V
BV_{EBO}	Emitter-Base Breakdown Voltage	$I_E = -100 \mu\text{A}$, $I_C = 0$	-6			V
I_{CBO}	Collector Cut-Off Current	$V_{CB} = -35 \text{ V}$, $I_E = 0$			-100	nA
I_{EBO}	Emitter Cut-Off Current	$V_{EB} = -6 \text{ V}$, $I_C = 0$			-100	nA
h_{FE1}	DC Current Gain	$V_{CE} = -1 \text{ V}$, $I_C = -5 \text{ mA}$	45	170		
h_{FE2}		$V_{CE} = -1 \text{ V}$, $I_C = -100 \text{ mA}$	85	160	300	
h_{FE3}		$V_{CE} = -1 \text{ V}$, $I_C = -800 \text{ mA}$	40	80		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = -800 \text{ mA}$, $I_B = -80 \text{ mA}$		-0.28	-0.50	V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	$I_C = -800 \text{ mA}$, $I_B = -80 \text{ mA}$		-0.98	-1.20	V
$V_{BE(on)}$	Base-Emitter On Voltage	$V_{CE} = -1 \text{ V}$, $I_C = -10 \text{ mA}$		-0.66	-1.00	V
C_{ob}	Output Capacitance	$V_{CB} = -10 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$		15		pF
f_T	Current Gain Bandwidth Product	$V_{CE} = -10 \text{ V}$, $I_C = -50 \text{ mA}$	100	200		MHz

 h_{FE} Classification

Classification	B	C	D
h_{FE2}	85 ~ 160	120 ~ 200	160 ~ 300

Typical Performance Characteristics

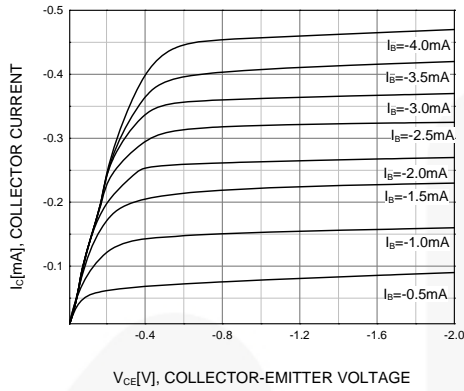


Figure 1. Static Characteristic

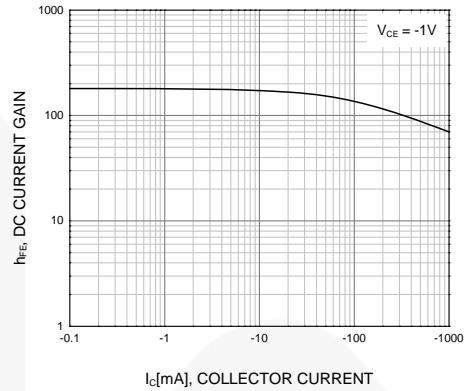


Figure 2. DC Current Gain

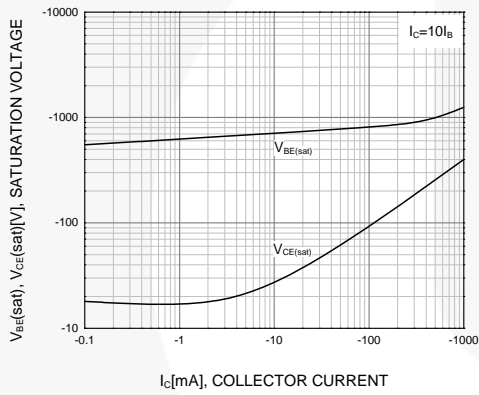


Figure 3. Base-Emitter Saturation Voltage and Collector-Emitter Saturation Voltage

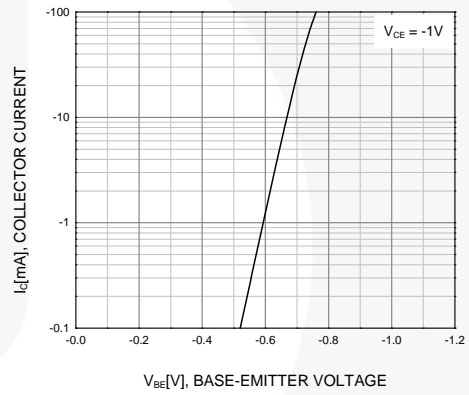


Figure 4. Base-Emitter On Voltage

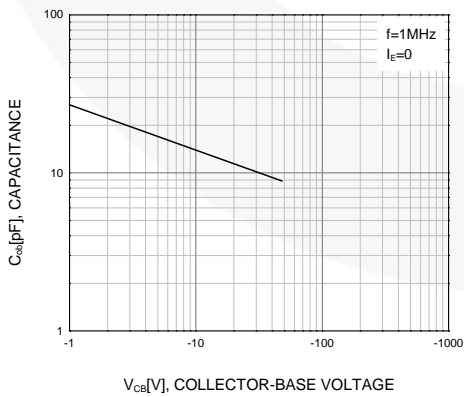


Figure 5. Collector Output Capacitance

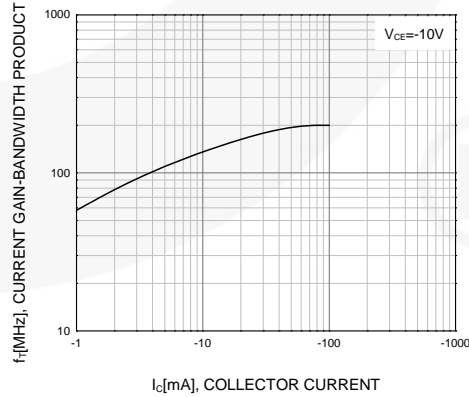
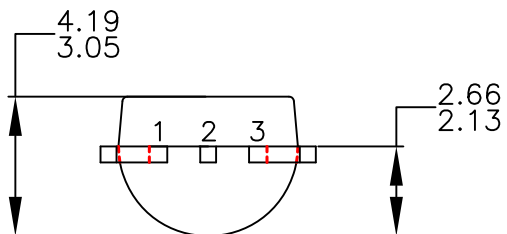


Figure 6. Current Gain Bandwidth Product



NOTES: UNLESS OTHERWISE SPECIFIED

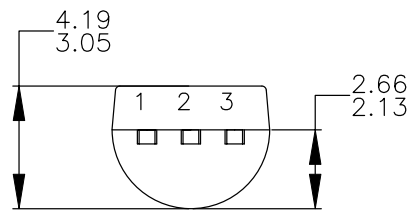
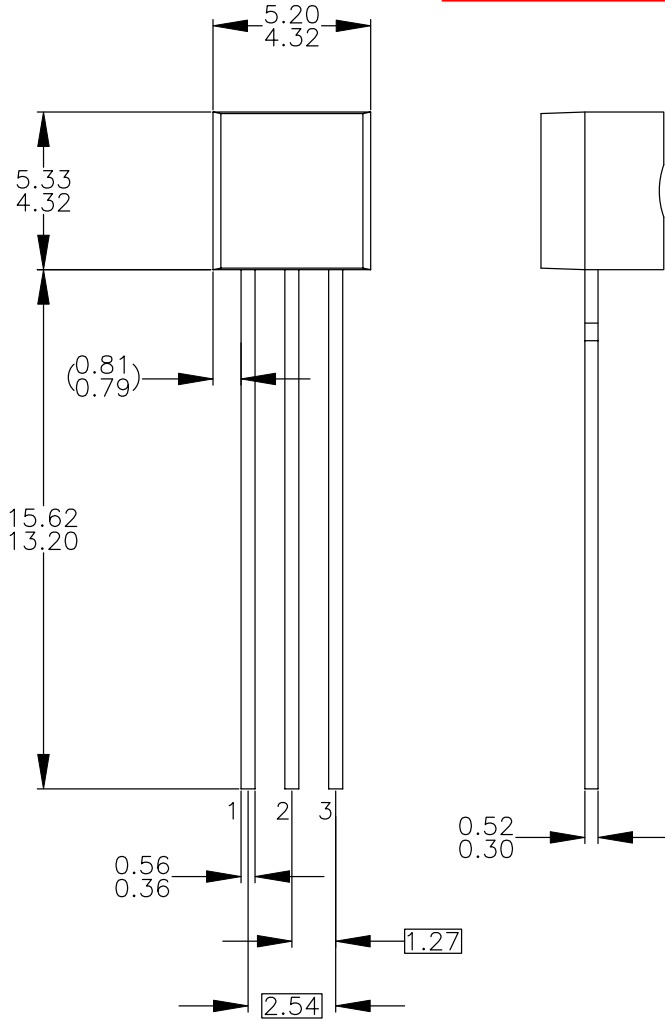
- A. DRAWING CONFORMS TO JEDEC MS-013, VARIATION AC.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5M-2009.
- D. DRAWING FILENAME: MKT-ZA03FREV3.
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APPROVED
July-14-2008

REVISIONS

NO.	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	MAR.4'96	RP
B	RDRW AS PER STD DWG TEMPLATE. CHG DIM REF FR DUAL DIM INCH(MM) TO SINGLE DIM MM. CHG LD PITCH DIM FR 1.14-1.40 TO 1.27 BSC. ADD DIM 2.54 BSC. CHG PKG WIDTH DIM FR 4.32- 4.70 TO 4.32-4.83; CHG PKG HEIGHT DIM FR 4.32-4.70 TO 4.32-4.78; CHG LD THICK DIM FR 0.30- 0.48 TO 0.30-0.52; DAMBAR-PKG DIM FR 1.27-1.65 TO 0.90-1.65; LD LGH DIM FR 14.47-15.64 TO 14.47-15.62; PKG DIM: 1.02-1.52 TO 0.92-1.52, 3.81-4.45 TO 3.40-4.80; NOTE 2: ADD DMOS "M" OPT'N AND LEGEND; NOTE B PKG 94 JFET OPT'N: CHG D TO S, CHG S TO D. ADD NOTE C. MOVE NOTE B INFO FR PKG 97&98 TO NEW NOTE D.	4OCT1999	RCM/MRG
3	CHG LD LEN FR 13.81 TO 13.80 ; CHG MOLD BODY HT FR 4.32 TO 4.32 ; CHG PKG EDGE TO LD EDGE DIST FR (0.81) TO (0.81); CHG MOLD BODY WIDTH FR 4.32 TO 4.32 ; ADD PKG THICKNESS DIM "E"; CHG "S" DIM FR 2.13 TO 2.13 ; REMOVE DAMBAR & EJECTOR PIN LOCATOR FEATURES & DIMENSIONS; REMOVE MOLDED SURFACE & DRAFT ANGLE DIMS; ADD NOTE ON JEDEC REFERENCE; ADD NOTE ON ASME Y14.5M-1994; REMOVE NOTE ON L34Z OPTION; ADD NOTE ON DWG FILENAME.	12FEB08	BMR/FSCP



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DRAWING CONFORMS TO ASME Y14.5M-1994.
 - D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P - BIPOLAR E - EMITTER D - DRAIN
F - JFET B - BASE S - SOURCE
M - DMOS C - COLLECTOR G - GATE

- E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEABLE AT JFET "F" OPTION.
- F) DRAWING FILENAME: MKT-ZA03DREV3.

APPROVALS	DATE	FAIRCHILD SEMICONDUCTOR™
DRAWN: J.U. COMPARATIVO JR.	03APR2008	
CHECKED: L. GALERA		
APPROVED: M.R. GESTOLE		
G.S. BAJE		3LD, TO-92, MOLDED STD STRAIGHT LD (NO EOL CODE)
PROJECTION 		SCALE: 1:1
INCH (MM)		SIZE: N/A
		DRAWING NUMBER: MKT-ZA03D
		REV: 3
		FORMERLY: N/A
		SHEET: 1 OF 1



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