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KA3525A

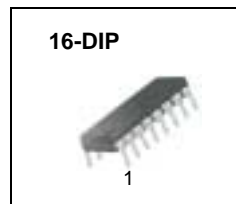
SMPS Controller

Features

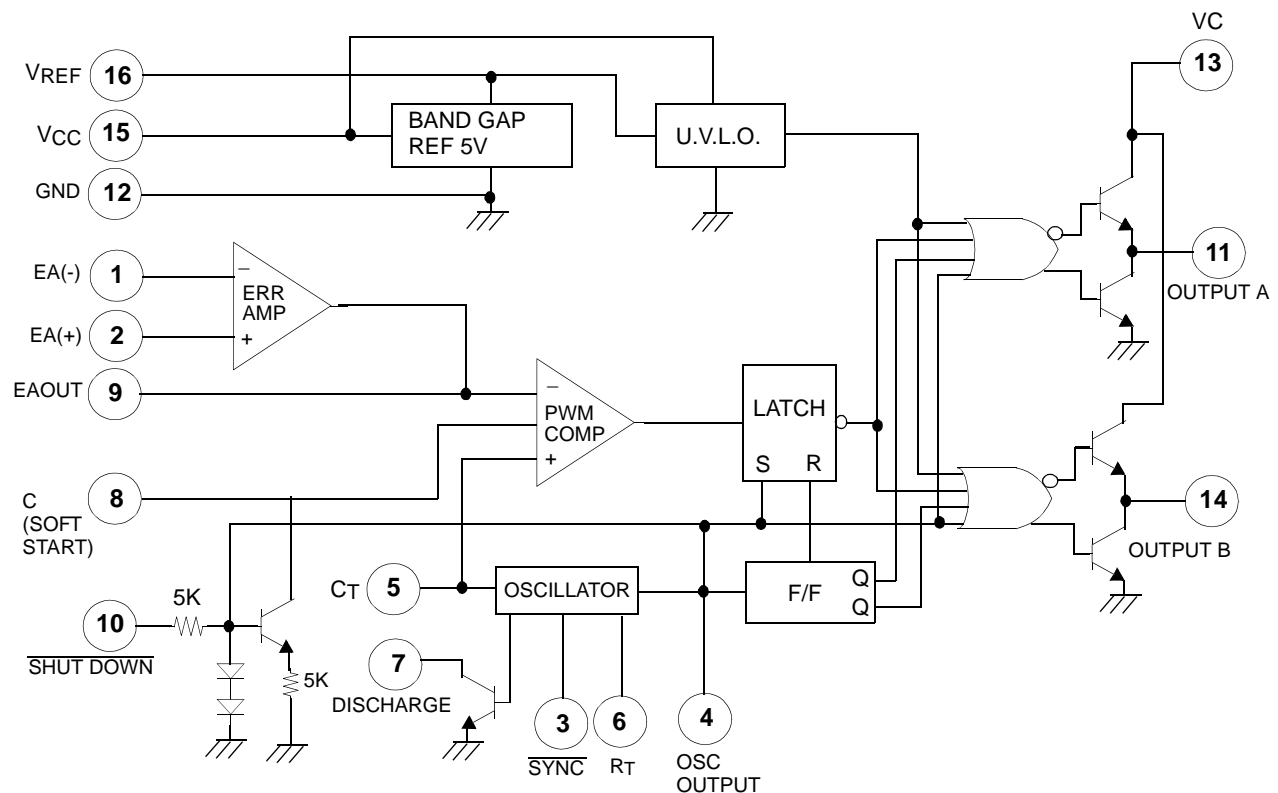
- 5V ±1% Reference
- Oscillator Sync Terminal
- Internal Soft Start
- Deadtime Control
- Under Voltage Lockout

Description

The KA3525A is a monolithic integrated circuit that includes all of the control circuits necessary for a pulse width modulating regulator. There are a voltage reference, an error amplifier, a pulse width modulator, an oscillator, an under voltage lockout, a soft start circuit, and the output driver in the chip.



Internal Block Diagram



Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|-----------------------|------------|------|
| Supply Voltage | VCC | 40 | V |
| Collector Supply Voltage | VC | 40 | V |
| Output Current, Sink or Source | IO | 500 | mA |
| Reference Output Current | IREF | 50 | mA |
| Oscillator Charging Current | I _{CHG(OSC)} | 5 | mA |
| Power Dissipation (T _A = 25°C) | P _D | 1000 | m/W |
| Operating Temperature | TOPR | 0 ~ +70 | °C |
| Storage Temperature | T _{STG} | -65 ~ +150 | °C |
| Lead Temperature (Soldering, 10sec) | T _{LEAD} | +300 | °C |

Electrical Characteristics

(VCC = 20V, T_A = 0 to +70°C, unless otherwise specified)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|--------------------------------|------------------------|--|------|------|------|------|
| REFERENCE SECTION | | | | | | |
| Reference Output Voltage | VREF | T _J = 25°C | 5.0 | 5.1 | 5.2 | V |
| Line Regulation | ΔVREF | VCC = 8 to 35V | - | 9 | 20 | mV |
| Load Regulation | ΔVREF | IREF = 0 to 20mA | - | 20 | 50 | mV |
| Short Circuit Output Current | ISC | VREF = 0, T _J = 25°C | - | 80 | 100 | mA |
| Total Output Variation (Note1) | ΔVREF | Line, Load and Temperature | 4.95 | - | 5.25 | V |
| Temperature Stability (Note1) | ST _T | - | - | 20 | 50 | mV |
| Long Term Stability (Note1) | ST | T _J = 125°C, 1KHS | - | 20 | 50 | mV |
| OSCILLATOR SECTION | | | | | | |
| Initial Accuracy (Note1, 2) | ACCUR | T _J = 25°C | - | ±3 | ±6 | % |
| Frequency Change With Voltage | Δf/ΔVCC | VCC = 8 to 35V (Note1, 2) | - | ±0.8 | ±2 | % |
| Maximum Frequency | f(MAX) | R _T = 2kΩ, C _T = 470pF | 400 | 430 | - | kHz |
| Minimum Frequency | f(MIN) | R _T = 200kΩ, C _T = 0.1uF | - | 60 | 120 | Hz |
| Clock Amplitude (Note1, 2) | V(CLK) | - | 3 | 4 | - | V |
| Clock Width (Note1, 2) | t _W (CLK) | T _J = 25°C | 0.3 | 0.6 | 1 | μs |
| Sync Threshold | V _{TH} (SYNC) | - | 1.2 | 2 | 2.8 | V |
| Sync Input Current | I _I (SYNC) | Sync = 3.5V | - | 1.3 | 2.5 | mA |

Electrical Characteristics (Continued)

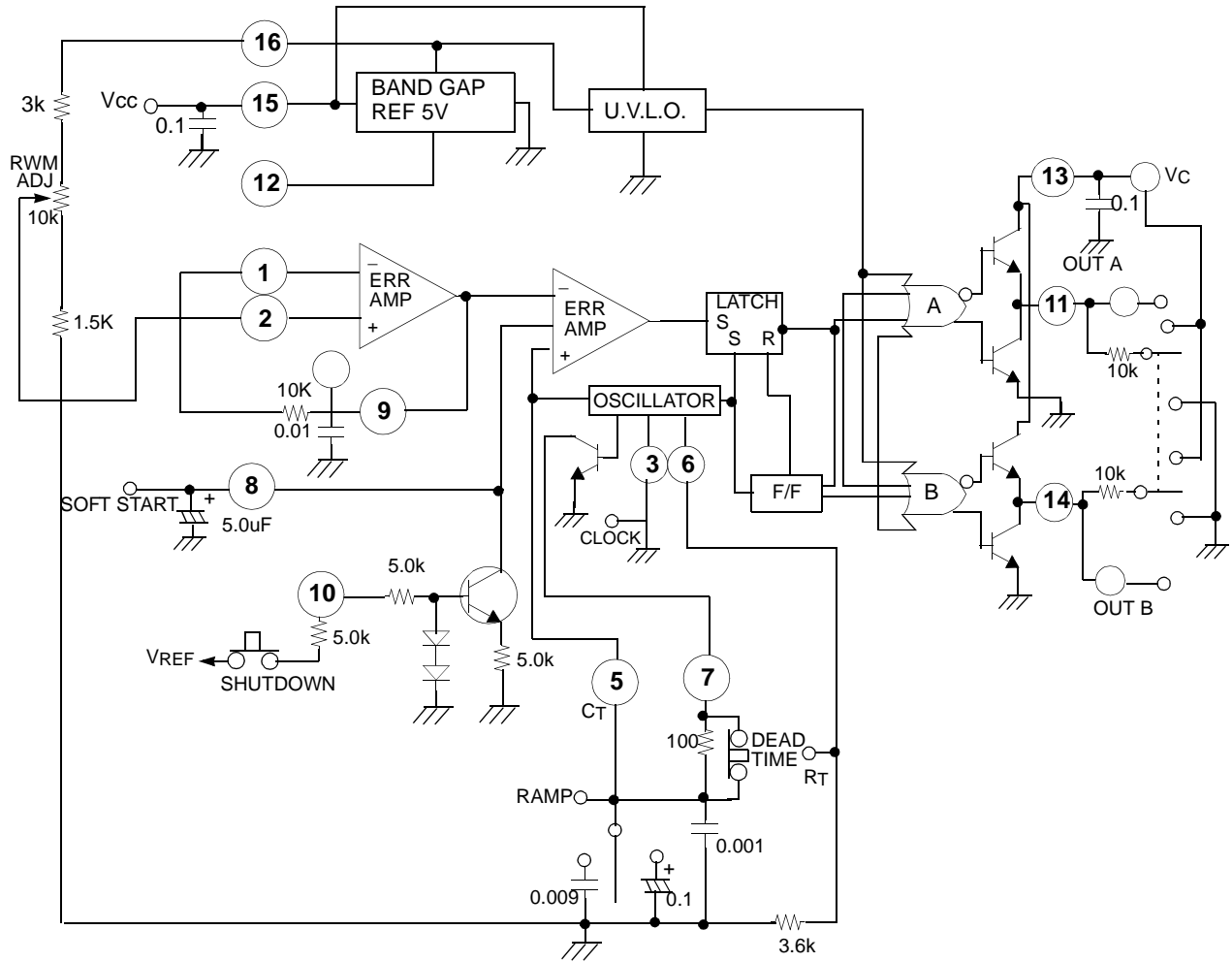
(VCC = 20V, TA = 0 to +70°C, unless otherwise specified)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|--|---------------------|---|------|------|------|------|
| ERROR AMPLIFIER SECTION (V_{CM} = 5.1V) | | | | | | |
| Input Offset Voltage | V _{IO} | - | - | 1.5 | 10 | mV |
| Input Bias Current | I _{BIAS} | - | - | 1 | 10 | μA |
| Input Offset Current | I _{IO} | - | - | 0.1 | 1 | μA |
| Open Loop Voltage Gain | G _{VO} | R _L ≥ 10MΩ | 60 | 80 | - | dB |
| Common Mode Rejection Ratio | CMRR | V _{CM} = 1.5 to 5.2V | 60 | 90 | - | dB |
| Power Supply Rejection Ratio | PSRR | V _{CC} = 8 to 3.5V | 50 | 60 | - | dB |
| PWM COMPARATOR SECTION | | | | | | |
| Minimum Duty Cycle | D(MIN) | - | - | - | 0 | % |
| Maximum Duty Cycle | D(MAX) | - | 45 | 49 | - | % |
| Input Threshold Voltage (Note2) | V _{TH1} | Zero Duty Cycle | 0.7 | 0.9 | - | V |
| Input Threshold Voltage (Note2) | V _{TH2} | Max Duty Cycle | - | 3.2 | 3.6 | V |
| SOFT-START SECTION | | | | | | |
| Soft Start Current | I _{SOFT} | V _{SD} = 0V, V _{SS} = 0V | 25 | 51 | 80 | μA |
| Soft Start Low Level Voltage | V _{SL} | V _{SD} = 25V | - | 0.3 | 0.7 | V |
| Shutdown Threshold Voltage | V _{TH(SD)} | - | 0.9 | 1.3 | 1.7 | V |
| Shutdown Input Current | I _{N(SD)} | V _{SD} = 2.5V | - | 0.3 | 1 | mA |
| OUTPUT SECTION | | | | | | |
| Low Output Voltage I | V _{OL I} | I _{SINK} = 20mA | - | 0.1 | 0.4 | V |
| Low Output Voltage II | V _{OL II} | I _{SINK} = 100mA | - | 0.05 | 2 | V |
| High Output Voltage I | V _{CH I} | I _{SOURCE} = 20mA | 18 | 19 | - | V |
| High Output Voltage II | V _{CH II} | I _{SOURCE} = 100mA | 17 | 18 | - | V |
| Under Voltage Lockout | V _{UV} | V ₈ and V ₉ = High | 6 | 7 | 8 | V |
| Collector Leakage Current | I _{LKG} | V _{CC} = 35V | - | 80 | 200 | μA |
| Rise Time (Note1) | t _R | C _L = 1μF, T _J = 25°C | - | 80 | 600 | ns |
| Fall Time (Note1) | t _F | C _L = 1μF, T _J = 25°C | - | 70 | 300 | ns |
| STANDBY CURRENT | | | | | | |
| Supply Current | I _{CC} | V _{CC} = 35V | - | 12 | 20 | mA |

Note :

1. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production
2. Tested at f_{OSC}=40kHz (R_T=3.6K, C_T=0.01μF, R_I = 0Ω)

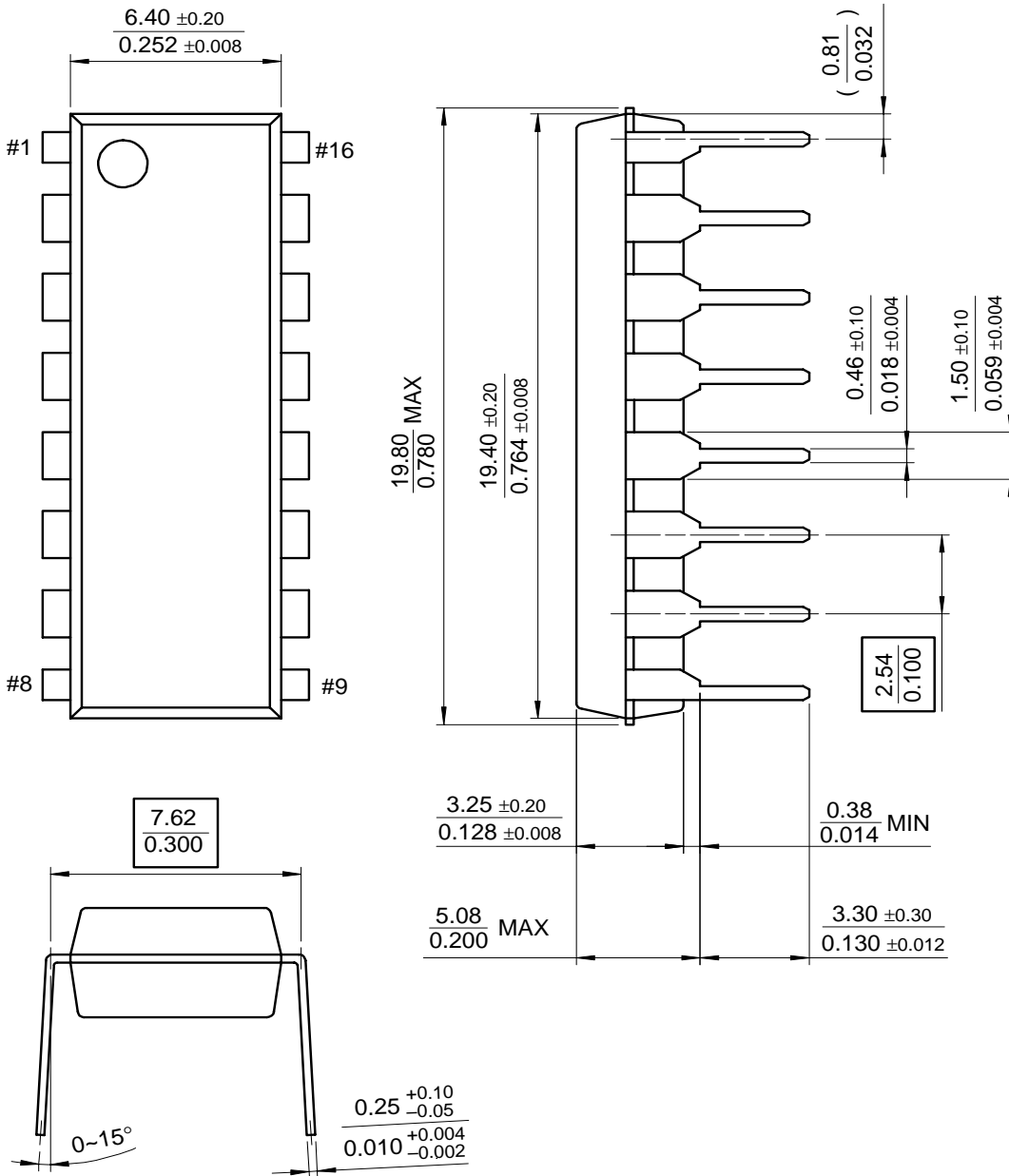
Test Circuit



Mechanical Dimensions

Package

16-DIP



Ordering Information

| Product Number | Package | Operating Temperature |
|----------------|---------|-----------------------|
| KA3525A | 16-DIP | 0 ~ +70°C |

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